System-Level Modeling and Simulation of the 10G Optoelectronic Interconnect

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***Abstract*—Mixed-signal multidomain systems present a challenge for computer-aided design tools. Optical and electronic simulation tools are available as separate entities. However, to date, successful system-level cosimulation has not been implemented, leading to expensive refabrication. We present a unique system-level simulation tool for mixed electrooptical systems. We apply our tool *Chatoyant* to the simulation of an optical high-speed free-space interconnect system designed for 10-GHz speeds. The 10G free-space optical interconnect module has optical, optoelectronic, and microwave components and thus is an ideal vehicle to use as a test system. We demonstrate how *Chatoyant,* a mixed-signal multidomain simulator, has been used to evaluate end-to-end performance of this complex system, including the exploration of design tradeoffs and mechanical tolerancing.**

***Index Terms*—Behavioral modeling, mixed-signal multidomain simulation, modified nodal analysis, piecewise linear simulation, system simulation of microsystems.**

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I. Introduction

THE 10G system [1] is a complex electrooptical interconnect that presents many challenges to a simulation environment. *Chatoyant* [2], [3] is a mixed-signal multidomain (MSMD) simulator created for systems like the 10G. In this paper, we demonstrate how an MSMD simulator like *Chatoyant* is used for design and verification of high-speed optoelectronic interconnects. We illustrate how Chatoyant can be:

a) used to calibrate models of components;
b) compared with existing computer-aided design tools designed to solve problems at one point in the design-abstraction/technology domain design space (e.g., SPICE for electronic circuit design);
c) used to explore the complex design tradeoffs found in electrooptical interconnects.

We begin by describing the 10G system and its ancestry in the FAST-Net project [4]. Next, we trace one path through the system, presenting how *Chatoyant* simulates each of the components in the system as well as comparing the simulation results against existing single domain simulators. We conclude by demonstrating the importance of interconnects on overall system performance as well as the role of mechanical tolerancing.

II. Interconnect System Overview

A. Introduction

Using free-space optical interconnection schemes, Nakahara *et al.* [5] showed that bandwidth densities of more than 1 Tb/s/cm^2 can be achieved with smart pixel arrays [6] (SPAs). The basic design of the free-space accelerator for switching terabit networks (FAST-Net) is a passive interconnection of an array of light emitters to an array of optical receivers for use as a multiprocessor interconnect fabric. The original FAST-Net optical system designed by Haney *et al.* [4] had a 4×4 array of mixed optoelectronic SPAs. Each SPA was a hybrid circuit with the CMOS driver/receiver chip bump bonded to the GaAs optoelectronic chip. These SPAs were designed to operate at a transmission speed of approximately 1 GHz, resulting in a total speed of $16\ \text{SPAs} \times 44\ \text{links/SPA} \times 1\ \text{Gb/link} = 704\ \text{Gb/s}$.

The 10G system, which we evaluate in this paper, is a second-generation version of FastNet. The electronics were

implemented in SiGe technology [7] instead of the CMOS circuitry of FastNet. Instead of the larger 4×4 array of FastNET, the 10G has a 2×2 array of SPAs. Each link in the system is designed to run at maximum of 10 GHz. Since there are nine emitters in each quadrant of each SPA, the total aggregate bandwidth (ignoring the loopback path) is 3 quadrants/SPA $\times$ 4 SPAs $\times$ 9 links/quadrant $\times$ 10 Gb/s/link $= 1080$ Gb/s.

B. System Design Aspects of the 10G

The physical design of the 10G system is shown in Fig. 1. The lenses are shown as gray cylinders above the electronics substrate. The top surface is a mirror. The ray path is illustrated schematically in Fig. 2.

The digital input is connected at the edge of the multichip module (MCM), which is wire-bonded to a SiGe-GaAs hybrid chip. The laser on the GaAs chip emits light upward toward the lens, which is reflected off a mirror and back through another lens and finally down to the detector circuitry. The digital outputs are wire-bonded at the edge of the MCM. Since the 10G was designed as an experimental testbed, each hybrid contains nine optoelectronic channels with different link electronics implemented in SiGe technology. Of these nine channels, only an asynchronous link was analyzed with the *Chatoyant* system. The clock for this link is sent over a different link and is recovered locally.

As shown in Fig. 3, each SPA contains four chips. The nine vertical cavity surface emitting lasers (VCSELs) and photodetector pairs in the hybrid circuit can communicate with the three other SPA's via the optical link. Due to the offset in the lens system, represented by the outline of the lens shown in Fig. 3, the optical path of the cluster closest to the center of the SPA is straight up to the mirror and back down to the same cluster, and therefore, no interconnect is made (and hence, no arrow is shown). The mapping of the other three clusters in each quadrant is shown with arrows. For example, using SPA0 (upper left), hybrid 0 communicates with itself, hybrid 1 communicates with SPA1 hybrid 0, hybrid 2 communicates with SPA2 hybrid 3, and hybrid 3 communicates with SPA3 hybrid 0.

In the 10G, each SPA is a hybrid circuit with SiGe driver/receivers bump bonded to 44 GaAs VCSEL emitters interleaved with 44 metal–semiconductor–metal (MSM) detectors as shown in Fig. 4.

Before discussing the simulation of the 10G, we discuss the simulation technology with particular emphasis on the mixed signal aspects.

III. Simulator Technology

A. Introduction

In MSMD simulators, there is a need for consistent modeling methodologies across domains and fast yet accurate simulation of systems at different abstraction levels. Fast simulation enables the user to perform system-level simulations easily and often, which permits the user to explore the effect of design tradeoffs at the system level. The simulator used for the 10G system, *Chatoyant*, is based on the Ptolemy [8] backplane and includes different simulators for the optical and electrical/mechanical components. Notably, because these simulators communicate through the same system-level simulator and use the same user interface, they present a unified view of simulation results. In the simulation of a system interconnect like the 10G, the typical simulation results are performance measures such as bit error rate (BER), eye diagrams, waveform plots, and signal-to-noise ratio (SNR) measurements. Next, we discuss the MSMD modeling methodologies.

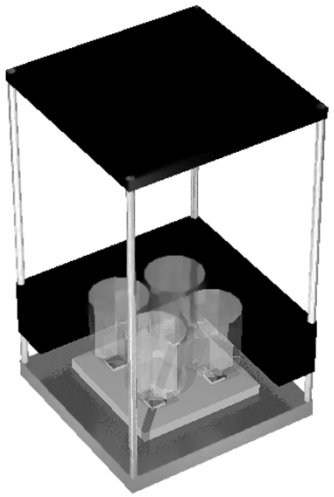

Fig. 1. Physical design of the 10G.

B. Behavioral Modeling

When choosing a modeling methodology for MSMD systems, we have to consider the types of interactions between components of different technologies. This depends on the the performance of the simulation environment, which depends on the simulation method and the type of signal characterization chosen. We can identify two different approaches to simulation as *behavioral modeling* and *equivalent circuit methods*.

Behavioral modeling is a flexible and general methodology that allows hierarchical support and mixed signal simulation. Typically, behavioral hardware description languages are extended to support analog signals (such as VHDL-AMS [9] or Verilog-A [10]) and are used to describe the system. Mixed-signal multidomain microsystems, which consist of a very large number of elements, produce a large computational load for typical mixed simulators, based on conventional analog simulators solving large sets of coupled differential equations.

Equivalent circuit methods use an equivalent circuit representation for the nonelectrical domain and then simulate this domain with any of established circuit simulators, e.g., SPICE [11] and iSmile [12]. iSmile was specifically designed for the simulation of electrooptical systems and includes flexible model definition as its primary feature. Together with a fiber-optics simulator iFrost [13], it was used to perform system-level simulations of an optical bus [14].

The lack of a common simulation backplane in simulators such as iSmile and iFrost means that communication between the two simulators is inconvenient at best. In addition, the equivalent circuit technique is limited by the lack of support for hierarchical design (since the circuit is flattened) and, because

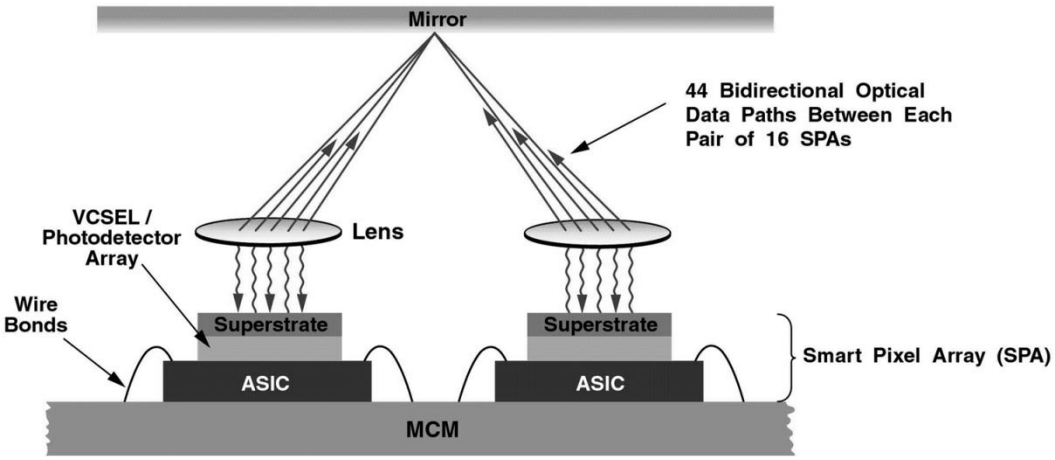

Fig. 2. Light path in the 10G.

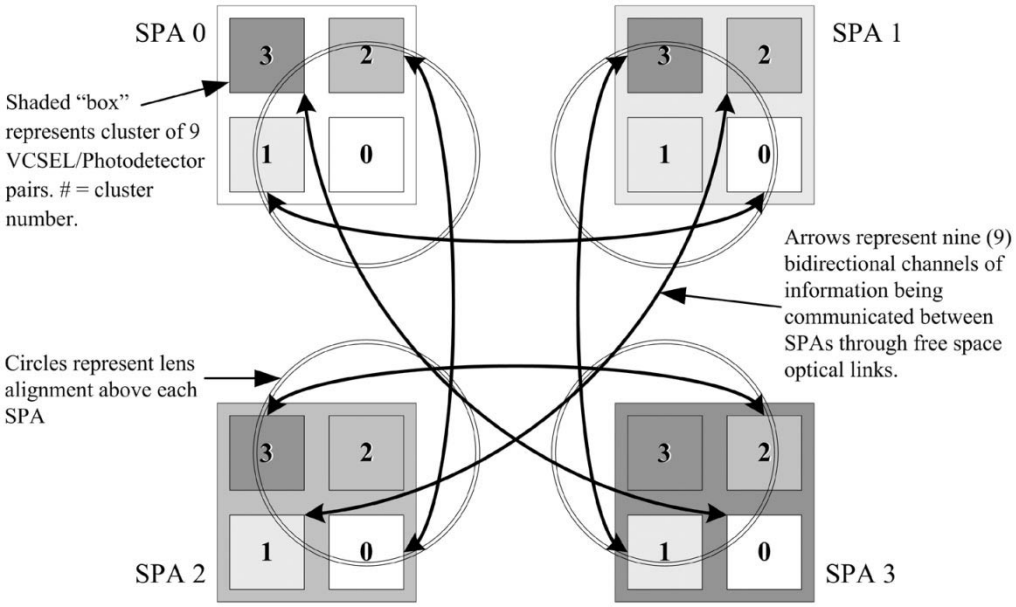

Fig. 3. SPA mapping.

the simulation is coupled to an analog simulator, digital simulation (i.e., binary values) is not performed. Therefore, digital simulations are performed using analog techniques, resulting in slow simulation time. In a system-level simulator like *Chatoyant*, the simulations must be fast, accurate, and convenient. In *Chatoyant*, SPICE circuit representations are used for electrical models *only* while different representations and simulators are used for other domains. All of them are integrated into one system simulation environment.

C. Piecewise Linear Modeling

In order to achieve simulation speedup, the heart of the analog simulator must be fast. As an alternative to traditional circuit simulation, nonlinear network modeling techniques using piecewise models have been developed [15], [16]. This technique has been applied in simulators such as NECTAR2 [17], PLANET [18], and PLATO [19]. These simulators are much more numerically stable when compared to traditional circuit simulators and provide flexibility for their use in hierarchical design. Conventional piecewise linear simulators use integration techniques to solve the transient response of the system since they are modeling continuous (analog) inputs. In *Chatoyant*, the piecewise linear technique was extended to also represent the discrete event signals. This has the advantage of eliminating the slowdown due to analog simulation of digital signals.

The center of the electrical simulator is a modified nodal analysis (MNA) solver [20], [21] that performs a linear analysis in the frequency domain. Since we are using a linear approximation, we decompose the multidimensional space of operating characteristics of active devices into regions each with a piecewise linear approximation. This gives us the ability to approximate the function to the degree of accuracy required for the

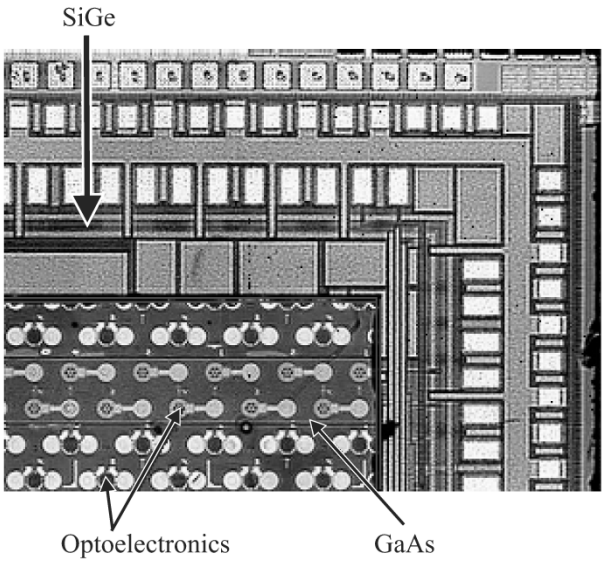

Fig. 4. Smart pixel array.

range of operation of interest. In addition, since many component models are written using SPICE syntax and semantics, a SPICE-like interface is provided. This enables the user to import existing SPICE netlists for electrical components while performing simulations with components from other domains (mechanical and optical). Linear components are added to the MNA matrix, whereas nonlinear components must be linearized by extracting linear regions of operation, as mentioned above. Next, the simulation of the 10G system with the MSMD modeling methodology will be detailed.

IV. Simulation of the 10G

The 10G transmission path is shown in Fig. 5. As shown, the incoming digital stream is connected to a pad on the edge of a MCM shown in Fig. 6. This pad is connected to a long transmission line that ends at a chip well for the SPA hybrid. A wire bond from the MCM signal layer is connected to the SiGe die. A short transmission line on the SiGe chip connects the pad to the driver/amplifier. A bump bond connects the SiGe substrate to the GaAs chip. The VCSEL emits light toward an offset lens system. The output of the lens reflects off the top mirror and back down to another lens. The output of the second lens is received by the MSM detector, which is connected via another bump bond to the SiGe receiver, which is composed of a transimpedance amplifier and a limiter. From this point, the receive path is the reverse of the transmission path.

In detail, this requires the following component models along the transmission path:

1) transmission line on the MCM from the input pad to the pad at the chip well edge (as shown in Fig. 6);
2) wirebond from the pad to the SiGe die on the SPA;
3) SiGe driver on the SPA die;
4) bump bond from the SiGe driver to the GaAs die;
5) VCSEL device on the GaAs die;
6) seven-element compound lens;
7) mirror;
8) seven element compound lens;

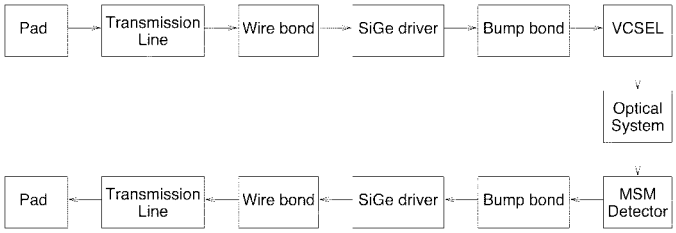

Fig. 5. 10G transmission path.

9) MSM device on the GaAs die;
10) bump bond from the MSM detector to the SiGe die;
11) transimpedance amplifier and limiter on the SPA die;
12) wirebond to the MCM pad;
13) transmission line on the MCM from the pad at the chip well edge to the output pad.

Subsequently, we show our modeling approach to each of these components.

A. Transmission Line

As shown in Fig. 6, the MCM is a multilayer laminate structure with ground and power planes interlaced throughout [22]–[24].

A similar laminate has also been used for an analog-to-digital converter running at 6 GHz [22]. Treating the ground planes as reference, we can use the dielectric constant of the signal plane to find the characteristic impedance. The transmission line can be modeled to different degrees of accuracy. Initially, the first model presented will be a simple lumped model of the entire line. The second model is a multisegment model.

The serpentine path of the asynchronous link signal trace can be obtained from a PCB layout tool. The first extraction of the asynchronous link (from pad to bond wire) is from the Cadence Allegro PCB tool [25]; the output is shown in the data in Table I.

Note that the impedance of the line has two values: the maximum impedance of any segment of a signal net and the minimum impedance of any segment of a signal net. We used the mean of these values as the overall line impedance. To form a lumped model, we constructed a T-network equivalent. The schematic of the lumped model is shown in Fig. 7.

This can be simulated using a time-domain electrical simulator such as Spectre-RF [26]. The simulation results are shown in the top two waveforms of Fig. 8. The *Chatoyant* simulation is shown in the bottom of the figure. Note that the Spectre-RF and *Chatoyant* simulations compare well. Also note how the waveform is distorted (the input is shown with a 100-ps risetime).

Using the multisegment data, the transmission lines can be converted into a geometric model suitable for either a multisegment lumped model or a three-dimensional full-wave finite-element simulation. In either case, the resulting scattering parameters can provide a frequency-dependent view of the line. The results from the multisegment microstrip model are shown in Fig. 9. Using this model in Agilent's ADS [27], the simulation of return loss benefits very little from the added complexity in the line model, though it is seen that the reflections decay earlier with the complex model (shown dipping below the simple model). The graph in Fig. 10 illustrates what happens when the transmission line is shorter: modes are easily visible. The

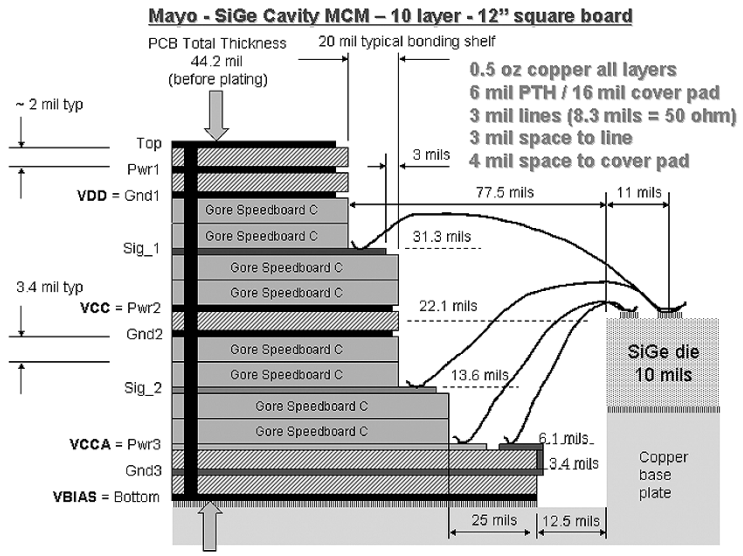

Fig. 6. SPA multilayer laminate structure.

TABLE I
CADENCE ALLEGRO LUMPED MODEL OUTPUT

Parameter	Description	Value
Z0	Impedance	57.962 ohm, 73.737 ohm
R	Resistance	188.773 mOhm
L	Inductance	23.8857 nH
Cg	Capacitance	14.1532 pF (to Shield Layer)
Cs	Capacitance	6.55227 pF (to signal)
Pd	Prop. Delay	0.822036 ns
Rterm	Termination	100 ohm

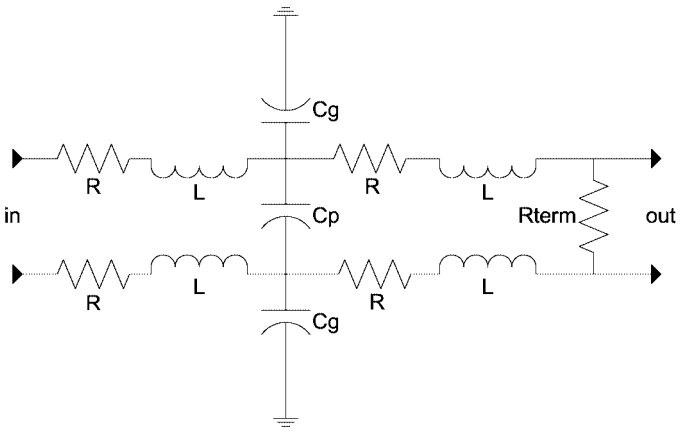

Fig. 7. Transmission-line lumped model schematic.

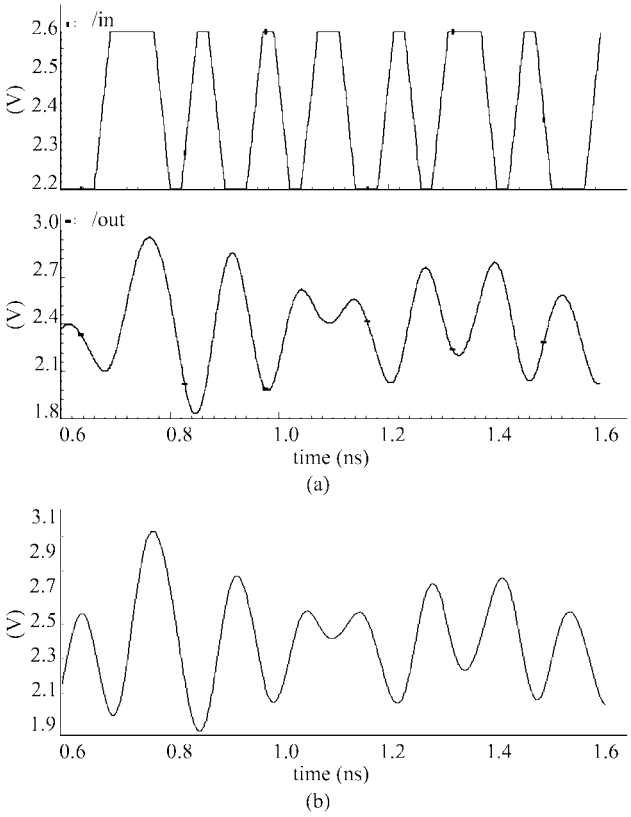

Fig. 8. Spectre-RF and *Chatoyant* lumped model simulation output.

simpler model (fewer segments) exhibits much deeper nulls, demonstrating the need for accurate transmission line models.

Complex microstrip models [28] are currently being added to *Chatoyant* so that fast multisegment models can be included in the simulation. Using full wave modeling, such as finite-difference time domain (FDTD) [29] or method of moments (MoM) [30], for the transmission line can increase simulation accuracy. However, in a behavioral simulator, these methods are neither fast enough for interactivity nor convenient due to the meshing requirement.

B. Wire Bonds

At microwave frequencies, wire bonds begin to affect signal integrity. There are two methods for modeling the bond wires: 1) mesh the wire and apply full wave methods like FDTD or MoM to calculate the S-parameters and 2) use a quasi-static model. The second approach turns out to be computationally easier and just as accurate. Alimenti *et al.* [31], [32] propose a simple model as follows: divide the bond wire into two halves;

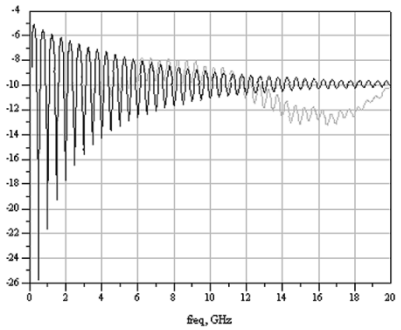

Fig. 9. Return loss transmission-line simulations using Agilent ADS for a long line.

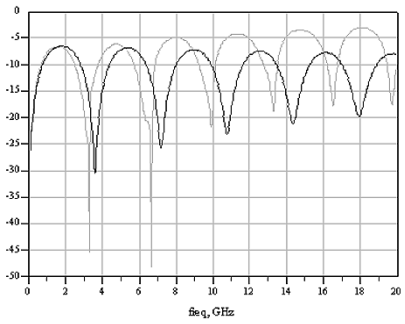

Fig. 10. Return loss transmission-line simulations using Agilent ADS for a short line.

each half is divided into three regions: the pad, the wire over the substrate, and then the wire over the ground plane, as shown in Fig. 11.

The pad is treated as a T-subcircuit and the other two regions as lossless transmission lines. The length of the transmission lines is computed by assuming that the bond wire is a radial chord. The T-subcircuit parameters are computed from lumped circuit assumptions.

The input parameters for the model of Alimenti *et al.* were determined by detailed examination of the MCM cross-section (Fig. 6). The equivalent circuit for the wire bond is shown in Fig. 12.

The component values for the equivalent T-subcircuits and transmission-line lengths were computed by a separate tool. The values shown in Table II gives the actual input parameters given to the tool derived by visual inspection of Fig. 6.

The generated SPICE output of the tool is shown in Table III. Note how the impedances (Z0) of the four transmission lines and the normalized length (NL) vary according to the different dielectrics. Using a 10-GHz input, the Spectre-RF and Chatoyant simulations are shown in Fig. 13.

The Spectre and *Chatoyant* waveforms differ slightly due to the use of the complex BSIM3 [33] models in Spectre. These models have more sophisticated high-frequency effects and are being currently added to *Chatoyant*.

C. SiGe Driver

A short transmission line connects the wirebond pad on the MCM to the SiGe chip with the VCSEL driver. The differential driver is composed of three stages: the input buffer, a limiter, and the source driver. The first step in modeling the SiGe circuit was linearizing the nonlinear behavior of the input/output characteristics. This was described previously in Section III-C. The

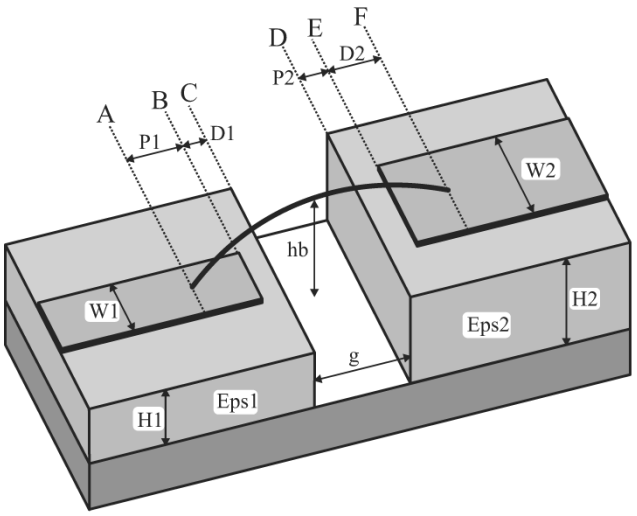

Fig. 11. Quasi-static bond wire model (from Alimenti *et al.* [32]).

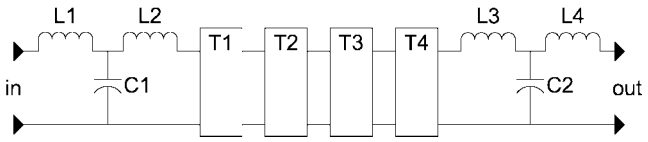

Fig. 12. Wire bond equivalent circuit model.

TABLE II
BOND WIRE PARAMETERS

Parameter	value	comments
W1	76.3	3 mil width
H1	795	31.3 mils
P1	254	10 mil pad
D1	76.2	3 mil separation
Eps1	4.4	
W2	254	10 mils
H2	561	22.1 mils high
D2	76.2	
Eps2	11.825	SiGe
hb	895	H1+4 mil height
g	317	12.5 mil gap
sw	25.4	1 mil wire

TABLE III
SPICE OUTPUT FROM BOND WIRE TOOL

```
L1 1 3 44.430311p
C2 3 2 0.045544p
L3 3 4 44.430311p
T1 4 2 6 7 Z0=256.61 F=10G NL=0.014910
T2 6 7 8 9 Z0=296.89 F=10G NL=0.003817
T3 8 9 10 11 Z0=294.88 F=10G NL=0.050158
T4 10 11 12 13 Z0=250.38 F=10G NL=0.014358
L8 12 14 17.492413p
C9 14 13 0.023994p
L10 14 15 17.492413p
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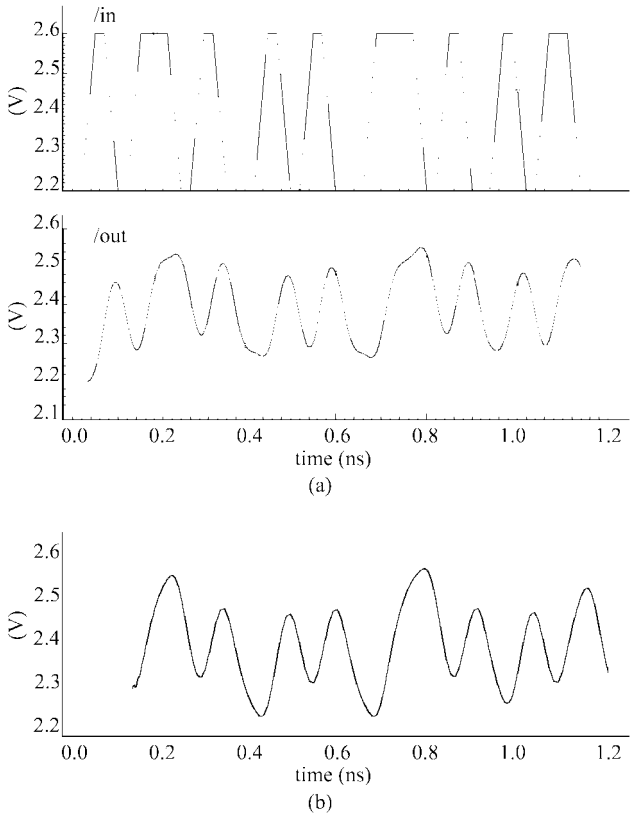

Fig. 13. Bond wire simulation: input, Spectre-RF, and *Chatoyant*.

output load is an ideal (DC) VCSEL model [34]. The output of the Spectre simulation is shown in Fig. 14 with the *Chatoyant* output directly below it.

D. Bump Bonds

The bump bond is the joint between the SiGe substrate and the GaAs optoelectronics. Bump bonds have been shown to be of great utility in microwave applications [35], [36]; however, they present an impedance discontinuity between substrates due to parasitic reactance [37]. Deriving an equivalent circuit for the solder bump is difficult, because it is hard to de-embed the bump from the substrates. One strategy is to use "design of experiments" [38] to obtain the equations for the components of the model. This was the approach taken by Staiculescu *et al.* [39]. They modeled the wire on the substrate as a coplanar waveguide (CPW) and used a standard π network. Using the CPW bump bond model, the following input parameters (all in mils, shown in Table IV) generates SPICE-compatible output directly usable by the *Chatoyant* simulator (shown in Table V).

E. VCSEL

At the other end of the solder bump is the laser (VCSEL). Most behavioral VCSEL models are DC models [40]–[42]. While DC models are useful for device characterization in the laboratory or fabrication line, they are inadequate when trying to characterize transient phenomena or high level behaviors. Our VCSEL model is a low-frequency piecewise linear (PWL) model, which includes temperature dependence and parasitics to account for the frequency response [5], [43].

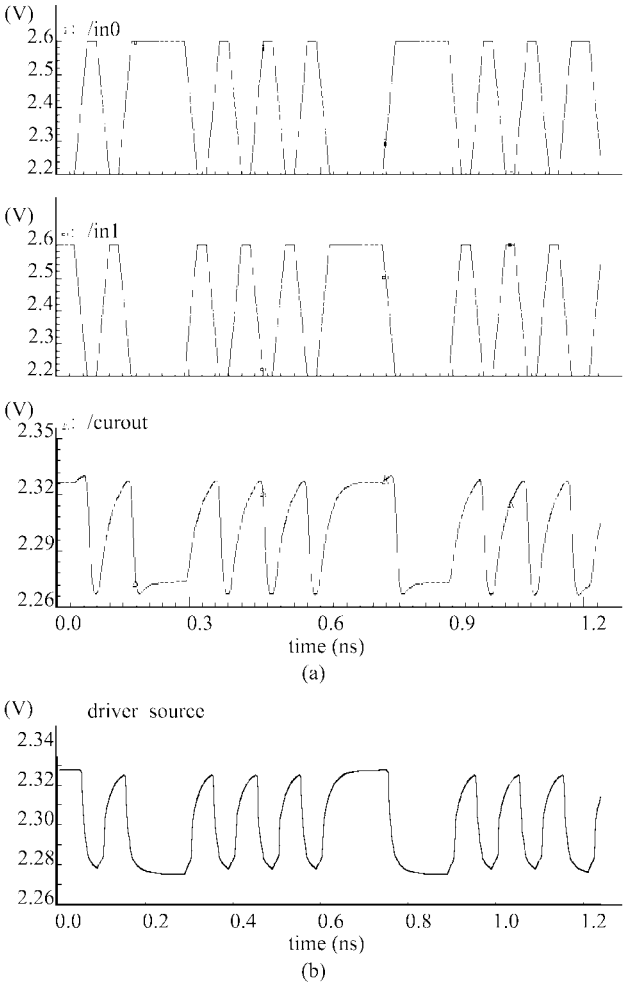

Fig. 14. Differential driver simulation.

TABLE IV
SOLDER BUMP PARAMETERS

Parameter	value (in mils)
Bump height	20
Conductor overlap	120
Width of line	150
Bump diameter	30
Distance to ground plane edge	50

TABLE V
SOLDER BUMP SPICE PARAMETERS

```
C1 1 2 18.859995f
L1 1 3 31.370040p
C2 3 2 18.859995f
```

The nonlinear behavior of this element is captured through a set of PWL regions of operation, as indicated in Fig. 15(a). Fig. 15(b) represents the circuit equivalent of this PWL model for the device. The mathematical definition of this model for the optical behavior of the VCSEL using four regions of operation is given by the equation at the bottom of the next page.

These expressions define the MNA to use in the simulation. The values of V_1, V_2, and V_3 are necessary to preserve conti-

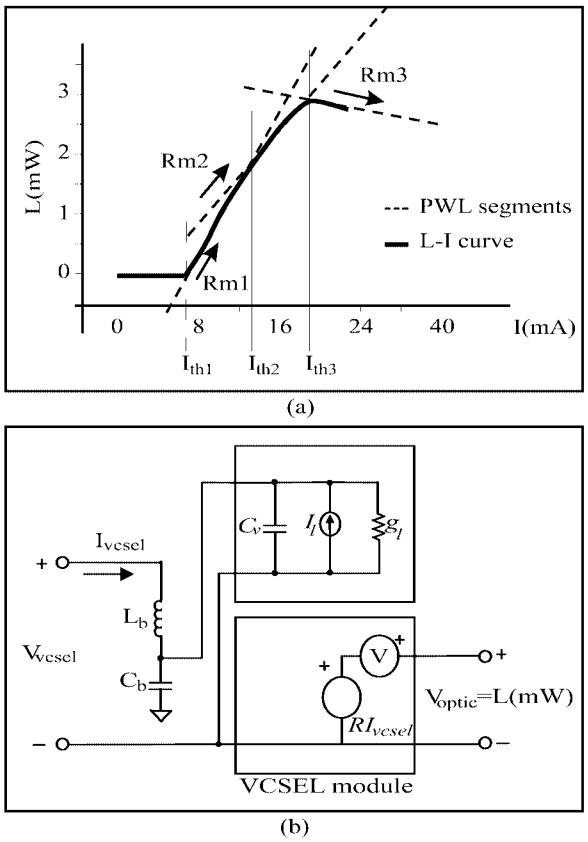

Fig. 15. (a) L–I curves for a VCSEL [44]. (b) PWL VCSEL model template.

nuity at the threshold values (I_{th}) chosen for the linearization. The transfer parameters Rm are dependent on the temperature of the VCSEL. The advantage of this characterization is that the designer can directly simulate the effects of electrical conditions in the VCSEL or associated driver against the optical power produced by this device. Additional dependencies can be added to the behavioral model following this approach (e.g, temperature, diameter of the VCSEL) that allows one to study their effect in complete system simulations. This behavioral model was compared against a lower level model derived from the rate equations and was found sufficient for high-level modeling purposes.

F. Compound Lens

Optical propagation based on Gaussian beam analysis allows paraxial light propagation to be modeled by nine scalar parameters and components to be modeled by an optical ABCD matrix [45]. This is opposed to simple ray-tracing analysis [46], [47], which is unable to model critical aspects of optical beams such as waist and intensity. The Gaussian parameters, in terms of optical waist, wavelength, intensity, and position, are initially set by the VCSEL parameters.

The optical propagation method used by the simulator is a mixture of ray analysis and Gaussian analysis. During propagation, the position and direction of the center of the Gaussian beam are calculated using typical ray methods. A Gaussian beam is superimposed over this ray-traced beam to model intensity, beam waist, phase, and depth of focus. The advantage of using Gaussian beam analysis is in the computational speed in which propagated light can be modeled. This permits interactive system-level design.

The complex lens used in the 10G system is the seven-element lens TK-11S from Universe Kogaku (America), Inc. Each interface between indexes of refraction of each lens element is modeled by the use of an ABCD matrix. From these interfaces, complete thick lens models are created and placed together to form doublets, triplets, and finally the complete complex lens. In the case of a spherical boundary between index of refractions n1 and n2, the ABCD values are: A$=1$, B$=0$, C$=-(n2-n1)/n2R$, D$=n2/n1$, where if R is a positive, the interface is convex, and if negative, the interface is concave. For propagation through a homogeneous dielectric medium, A$=1$, B$=d$, C$=0$, and D$=1$, where d is the distance of propagation. Using these interfaces, thick lens models are created, with a spherical boundary, a distance of propagation, and another spherical interface. The final model was composed of seven separate lens models. Using this complete lens model, we have been able to simulate the 10G optical subsystem and make many observations about the positioning and tolerancing of the system. We have determined that the distance between the substrate (VCSEL/MSM) and the lenses dominates the magnification of the VCSEL array on the MSM plane. The distance between the lenses and the mirror controls the focus of the VCSEL spots on the detectors. We have also shown that a slight lateral misalignment (i.e., not in the optical path) of the lenses is acceptable, and the optical power detected on the detector falls off -3 dB with a misalignment of approximately 40 μm, as shown in Fig. 16.

G. Mirror

The mirror is modeled as being perfectly flat (i.e., no curvature and no surface roughness) and 100% reflective but perfect mechanical alignment is *not* assumed. As the simulation shows in Fig. 17, the mirror alignment, especially the mirror tilt, is critical to the performance of the system.

H. MSM Detector

Continuing along the light path, the wavefront reflects off the mirror and propagates through another lens to the optical de-

$$V_{\text{output}} = \begin{cases} R_{m3}I - V_3 & I > I_{th3} \\ R_{m2}I - V_2 & I > I_{th3} \\ R_{m1}I - V_1 & I > I_{th3} \\ 0 & I < I_{th3} \end{cases} \quad \begin{array}{l} V_1 = R_{m1}I_{th1} \\ V_2 = R_{m2}I_{th2} - R_{m1}(I_{th2} - I_{th1}) \\ V_3 = R_{m3}I_{th3} - R_{m2}\,(I_{th3} - I_{th2}) - R_{m1}(I_{th2} - I_{th1}) \end{array}$$

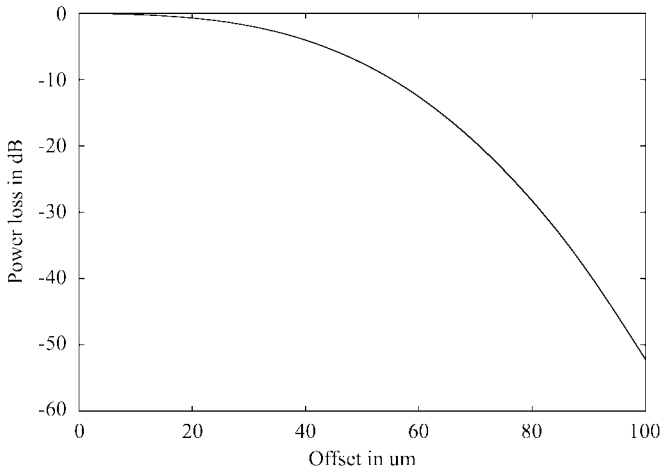

Fig. 16. Power loss due to lens offset.

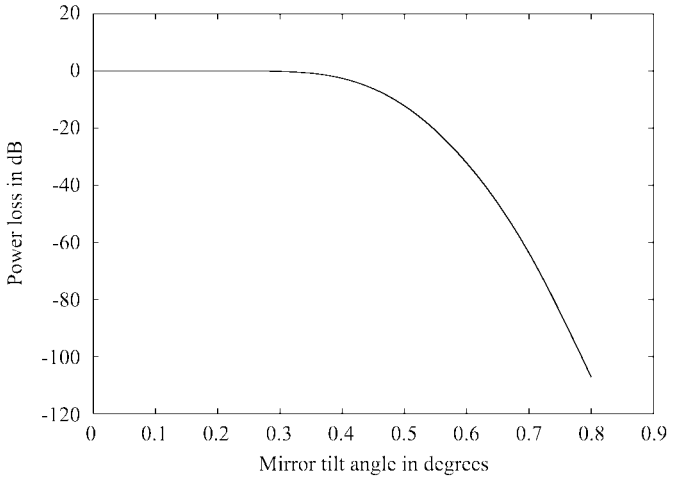

Fig. 17. Power loss due to mirror tilt.

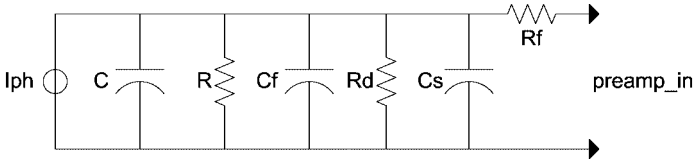

Fig. 18. First-order MSM detector model.

tector as shown in Fig. 2. Optical detection can be carried out with a photodiode, such as a PIN diode or by an MSM detector. The 10G system uses an MSM detector on the GaAs die. We characterize the behavior of the detector as a first-order system model [48], shown in Fig. 18. The standard model to describe this element is given by a current source I_{ph} to characterize the detected optical power and the dark current effect in parallel with a capacitor C and resistance R to characterize the transit time in the device. To account for the dynamic response of the element to high frequencies, lumped parasitics are also included. These parasitics correspond to resistances of the MSM fingers (R_f), the bulk resistance (R_b), capacitance between the substrate and the semiconductor (C_s), and capacitance between fingers (C_f).

This model is not complete and in particular is missing noise source models, which become critical when the received signal is low level. In the short-range system described here, this is not a problem.

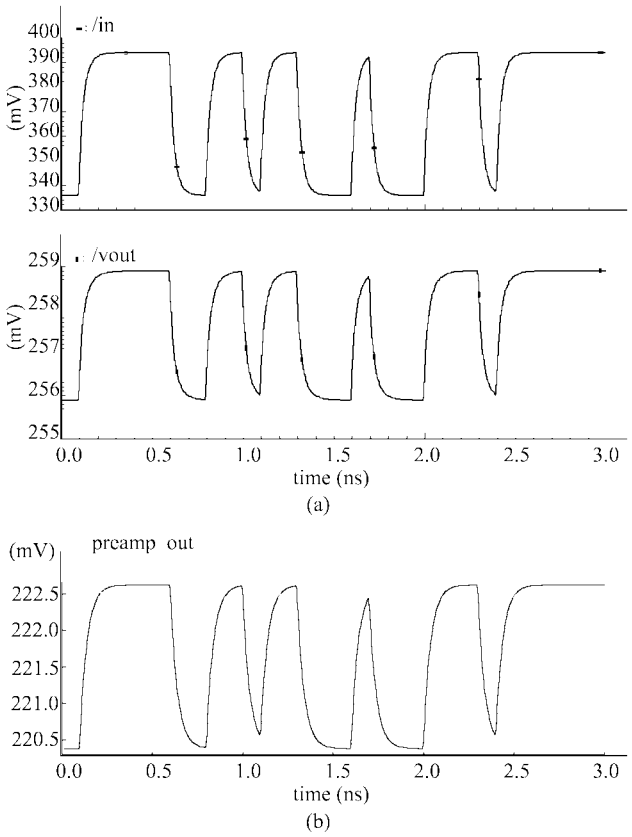

Fig. 19. Spectre and *Chatoyant* simulations of the SiGe receiver.

I. SiGe Receiver

After the bump bond is a short transmission line from the SiGe chip to the receiver. The multistage receiver has a transimpedance amplifier first stage, followed by a buffer, a three-stage low-noise amplifier, and finally a limiter. The output of the receiver pad is connected to the wirebond and back out to the output pad. Again, these were simulated with *Chatoyant* and compared against the Spectre simulations, as shown in Fig. 19.

V. Results

Using the models above, we can simulate the system end-to-end. The parameters of these models can be changed and the simulations rerun. Because these are higher level models, the simulation time is on the order of seconds, not hours. For example, an end-to-end simulation can be run on the entire system as shown below as input and output pairs (in Fig. 20). This presents the performance results of the whole system, so the designer can get fast evaluation of the feasibility of the design under consideration. *Chatoyant* can be used to generate graphical measures of system performance, such as eye diagrams. Additionally, quantitative measurements such as BER are calculated through statistical estimation [48]. We can see the eye openings with a 2.5-GHz input (shown in Fig. 21). At 5.0 GHz, the eye opening significantly degrades, as shown in Fig. 22.

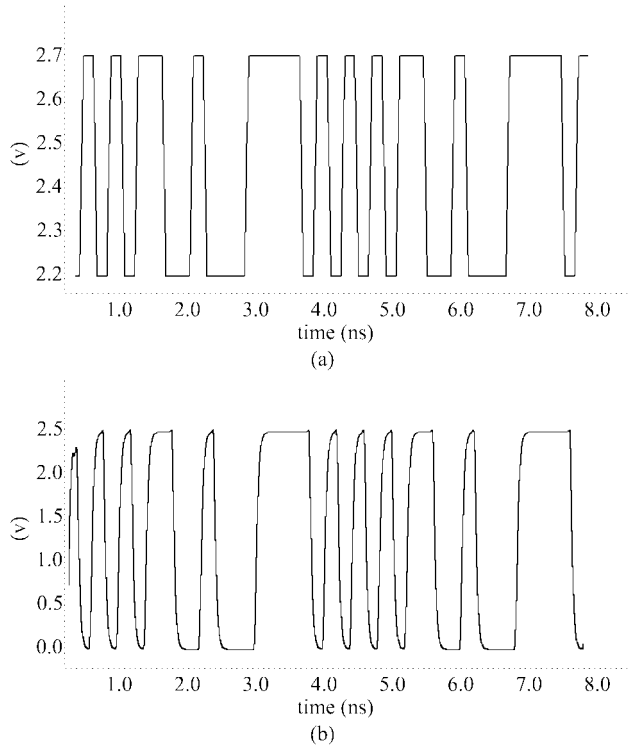

Fig. 20. *Chatoyant* system output observed at the input and output pad.

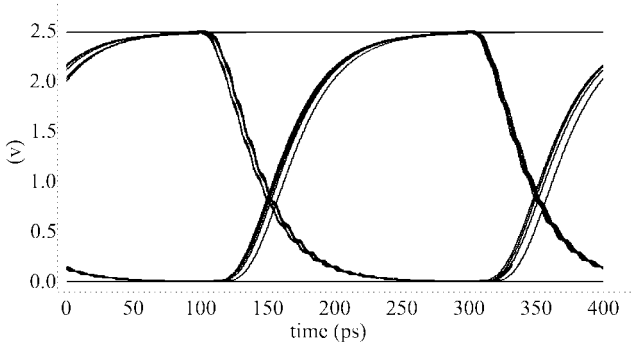

Fig. 21. Eye opening at 2.5 GHz.

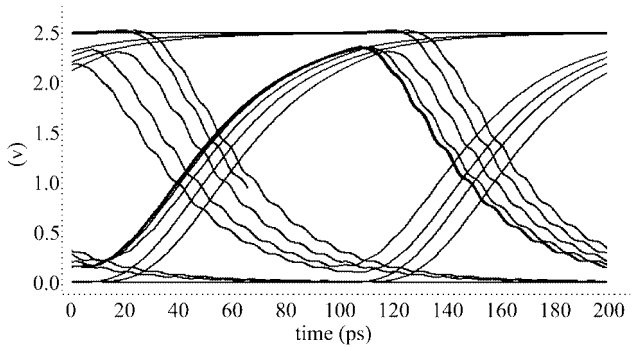

Fig. 22. Eye opening at 5.0 GHz.

Additional tests can be performed on mechanical tolerancing, which is critical to optoelectronic systems. Here, a 45-μm SPA offset leads to the eye opening shown in Fig. 23. A 15-μm lens offset in X or Y is shown in Fig. 24.

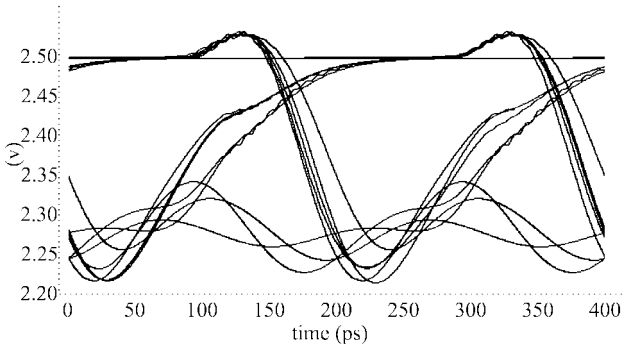

Fig. 23. Eye opening with SPA offset in X or Y.

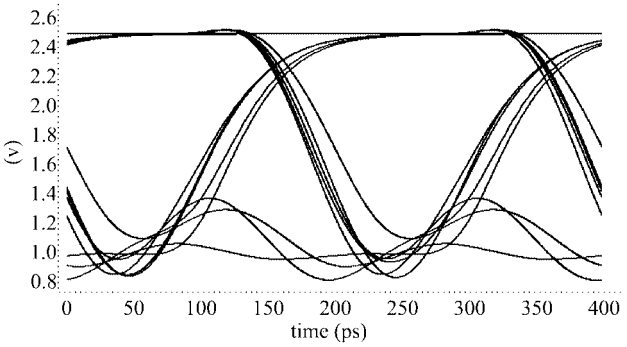

Fig. 24. Eye opening with lens offset in X or Y.

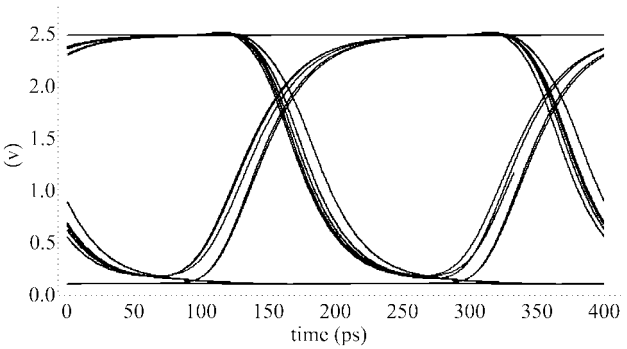

Fig. 25. Eye opening with lens offset in Z.

Note that in the Z-direction (out of the plane), the eye is not nearly as sensitive. For a 250-μm offset in Z, the eye is shown in Fig. 25.

VI. Conclusion

The ability to perform "what-if" studies is compelling because it is faster and costs significantly less than fabrication and also provides ease in modeling new devices and interconnect structures. Although this example models a system in construction (the 10G), it demonstrates that it will be difficult to achieve the full design speed of 10 GHz. Furthermore, it also points out the need for careful attention to the signal integrity issues of transmission-line design on the hybrid as well as the importance of critical mechanical tolerancing. It also provides a uniform simulation environment to explore system performance. The *Chatoyant* simulator is able to perform these complete system simulations because of new models

of electrooptical components, a new PWL/MNA solver for electrical components, and fast Gaussian light propagation all coupled together using a common simulation framework.

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REFERENCES

[1] G. J. Fokken, W. L. Walters, L. F. Mattson, and B. K. Gilbert, "Low-cost, multi-GHz electrical packaging for serial optoelectronic links utilizing vertical cavity surface, emitting lasers," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 42–54, Feb. 2000.

[2] S. P. Levitan, T. P. Kurzweg, P. J. Marchand, M. A. Rempel, D. M. Chiarulli, J. A. Martínez, J. M. Bridgen, C. Fan, and F. B. McCormick, "Chatoyant: a computer-aided- design tool for free-space optoelectronic systems," *Appl. Opt. Inform. Process.*, vol. 37, no. 26, pp. 6078–6092, Sept. 1998.

[3] S. P. Levitan, J. A. Martinez, T. P. Kurzweg, A. J. Davare, M. Kahrs, and D. M. Chiarulli, "System simulation of mixed-signal multi-domain microsystems with piecewise linear models," *IEEE Trans. Computer-Aided Design*, vol. 22, pp. 139–154, Feb. 2003.

[4] M. W. Haney, M. P. Christensen, P. Milojkovic, G. J. Fokken, M. Vickberg, B. K. Gilbert, J. Rieve, J. Ekman, P. Chandramani, and F. Kiamilev, "Description and evaluation of the FAST-Net smart pixel-based optical interconnection prototype," *Proc. IEEE*, vol. 88, no. 6, pp. 819–828, June 2000.

[5] T. Nakahara, S. Matsuo, S. Fukushima, and T. Kurokawa, "Performance comparison between multiple-quantum-well modulator-based and vertical-cavity-surface-emitting laser-based smart pixels," *Appl. Opt. Inform. Process.*, vol. 35, no. 5, pp. 860–871, Feb. 1996.

[6] Y. Liu, "Heterogeneous integration of OE arrays with Si electronics and microoptics," *IEEE Trans. Adv. Packag.*, vol. 25, p. 43, Feb. 2002.

[7] K. E. Fritz, B. A. Randall, G. J. Fokken, W. L. Walters, M. J. Lorsung, A. D. Nielsen, J. F. Prairie, D. J. Post, D. R. Greenberg, and B. K. Gilbert, "High-speed, low-power digital and analog circuits implemented in IBM SiGe BiCMOS technology," in *21st Annu. GaAs IC Symp.*, vol. 21, 1999, pp. 41–44.

[8] J. T. Buck, S. Ha, E. A. Lee, and D. G. Messerschmitt, "Ptolemy: a framework for simulating and prototyping heterogeneous systems," *Int. J. Comput. Simulat. (Special Issue on Simulation Software Development)*, vol. 4, pp. 155–182, Apr. 1994.

[9] *IEEE Standard VHDL, Language Reference Manual (Integrated with VHDL-AMS Changes)*, IEEE, 1997.

[10] *Verilog-A: Language Reference Manual*, Open Verilog International, 2001.

[11] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," University of California, Berkeley, Electronic Research Lab. Rep. ERL-M75/520, May 1975.

[12] A. T. Yang and S. M. Kang, "iSMILE: a novel circuit simulation program with emphasis on new device model development," in *Proc. 26th ACM/IEEE Design Automation Conf.*, 1989, pp. 630–633.

[13] B. K. Whitlock, P. K. Pepeljugoski, D. M. Kuchta, J. D. Crow, and S.-M. Kang, "Computer modeling and simulation of the Optoelectronic Technology Consortium (OETC) optical bus," *IEEE J. Select. Areas Commun.*, vol. 15, pp. 717–730, May 1997.

[14] B. K. Whitlock, J. J. Morikuni, E. Conforti, and S.-M.Sung-Mo Kang, "Simulation and modeling: simulating optical interconnects," *IEEE Circuits Devices Mag.*, vol. 11, no. 3, pp. 12–18, May 1995.

[15] R. Kao and M. Horowitz, "Timing analysis for piecewise linear RSIM," *IEEE Trans. Computer-Aided Design*, vol. 13, pp. 1498–1512, Dec. 1994.

[16] A. Salz and M. Horowitz, "IRSIM: An incremental MOS switch-level simulator," in *Proc. 26th Design Automation Conf.*, 1989, pp. 173–178.

[17] K. Kawakita and T. Ohtsuki, "NECTAR2—circuit analysis program based on piecewise linear approach," in *Proc. ISCAS*, 1975, pp. 92–95.

[18] M. H. Zaman, S. F. Bart, J. R. Gilbert, N. R. Swart, and M. Mariappan, "An environment for design and modeling of electro-mechanical microsystems," *J. Model. Simulat. Microsyst.*, vol. 1, no. 1, pp. 65–76, 1999.

[19] D. M. W. Leenaerts and W. M. G. Bokhoven, *Piecewise Linear Modeling and Analysis*. Norwell, MA: Kluwer Academic, 1998.

[20] P. Feldmann and R. W. Freund, "Efficient linear circuit analysis by Padé approximation via the Lanczos process," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 639–649, May 1995.

[21] J. A. Martínez, T. P. Kurzweg, S. P. Levitan, P. J. Marchand, and D. M. Chiarulli, "Mixed-technology system-level simulation," *Analog Integrat. Circuits Signal Process.*, vol. 29, pp. 127–149, Oct./Nov. 2001.

[22] D. J. Schwab, B. Randall, P. J. Zabinski, T. M. Schaefer, and B. K. Gilbert, "The use of laminate multichip modules for the packaging of 9-GHz digital multichip circuits," *IEEE Trans. Adv. Packag. B*, vol. 25, pp. 79–91, Feb. 2002.

[23] B. Gilbert, R. Thompson, G. Fokken, W. McNeff, J. Prentice, D. Rowlands, A. Staniszewski, W. Walters, S. Zahn, and G. W. Pan, "Advanced multichip module packaging and interconnect issues for GaAs signal processors operating above 1 GHz clock rates," in *Proc. SPIE Microelectronic Interconnects Packages—System and Process Integration, Pt. 2*, vol. 1390, Nov. 1990, pp. 235–248.

[24] B. K. Gilbert, M. J. Degerstrom, P. J. Zabinski, T. M. Schafer, G. J. Fokken, B. A. Randall, D. J. Schwab, E. S. Daniel, and S. C. Sommerfeldt, "Emerging multigigahertz digital and mixed-signal integrated circuits targeted for military applications: dependence on advanced electronic packaging to achieve full performance," *Proc. IEEE*, vol. 89, no. 4, pp. 426–443, April 2001.

[25] *Allegro PCB User's Manual*, Cadence, 2002.

[26] K. S. Kundert, *A Designer's Guide to Spice and Spectre*: Kluwer, 1995.

[27] *Agilent ADS User's Manual*: Agilent, 2002.

[28] K. C. Gupta, R.Ramesh Garg, I.Inder Bahl, and P.Prakash Bhartia, *Microstrip Lines and Slotlines*, 2nd ed. Reading, MA: Artech House Microwave Library, Mar. 1996.

[29] A. Taflove and S. Hagness, *Computational Electrodynamics: The Finite-Difference Time-Domain Method*, 2nd ed. Reading, MA: Artech House, 2000.

[30] R. F. Harrington, *Field Computation by Moment Methods*. New York: Wiley-IEEE Press, Apr. 1993.

[31] F. Alimenti, U. Goebel, and R. Sorrentino, "Quasi static analysis of microstrip bondwire interconnects," in *IEEE MTT-S Dig.*, 1995, pp. 679–682.

[32] F. Alimenti, P. Mezzanotte, L. Roselli, and R. Sorrentino, "Modeling and characterization of bonding-wire interconnection," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 142–150, Jan. 2001.

[33] "BSIM3 Version 3.1 User's Manual," Univ. of California at Berkeley, 1997.

[34] F. E. Kiamilev and A. V. Krishnamoorthy, "A high-speed 32-channel CMOS VCSEL driver with built-in self-test and clock generation circuitry," *IEEE J. Select. Topics Quantum Electron.*, vol. 5, no. 2, pp. 287–295, 1999.

[35] M. Case, "SiGe MMIC's and flip-chip MIC's for low-cost microwave systems," in *1997 IEEE RF Integrated Circuits Symp.*, 1997, pp. 117–120.

[36] H. H. M. Ghouz and E. B. El-Sharawy, "An accurate equivalent circuit model of flip chip and via interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2543–2554, Dec. 1996.

[37] G. A. Rinne and P. D. Franzon. The parasitic reactances of flip chip solder bumps. [Online]http://www.unitive.com/casestudies/pdfs/par.pdf

[38] D. C. Montgomery, *Design and Analysis of Experiments*. New York: Wiley, 1996.

[39] D. Staiculescu, A. Sutono, and J. Laskar, "Wideband scalable electrical model for microwave/millimeter wave flip chip interconnects," *IEEE Trans. Adv. Packag.*, vol. 24, pp. 255–259, Aug. 2001.

[40] J. Deng, M. S. Shur, T. A. Fjeldly, and S. Baier, "CAD tools and optical device models for mixed electronic/photonic VLSI," *Int. J. High Speed Electron. Syst.*, vol. 10, no. 1, pp. 299–308, 2000.

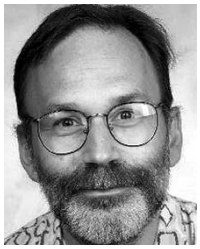
[41] J. Deng, "Characterization and modeling of advanced electronic and optoelectronic devices," Ph.D. dissertation, Rensselaer Polytechnic Inst., Troy, NY, 2001.

[42] A. Xiang, W. Wohlmuth, P. Fay, S. Kang, and I Adesida, "Modeling of InGaAs MSM photodetctor for circuit-level simulation," *J. Lightwave Technol.*, vol. 14, pp. 716–723, May 1996.

[43] C. Fan, B. Mansoorian, D. A. Van Blerkom, M. W. Hansen, V. H. Ozguz, S. C. Esener, and G. C. Marsden, "Digital free-space optical interconnections: a comparison of transmitter technologies," *Appl. Opt. Inform. Process.*, vol. 34, no. 17, pp. 3103–3115, June 1995.

[44] O. Kibar, D. Van Blerkom, C. Fan, P. J. Marchand, and S. C. Esener, "Small signal equivalent circuits for a semiconductor laser," *Appl. Opt. Inform. Process.*, vol. 37, no. 26, pp. 6136–6139, Sept. 1998.

[45] M. Born and E. Wolf, *Principles of Optics: Electromagnetic Theory of Propagation, Interference and Diffraction of Light*, 7th ed. Cambridge, U.K.: Cambridge Univ. Press, Dec. 1999.
[46] M. P. Christensen, P. Milojkovic, and M. W. Haney, "Aberration analysis of beam-steering in the FAST-Net global interconnection system," in *Lasers and Electro-Optics Society 13th Annu. Meeting (LEOS 2000)*, vol. 1, Nov. 2000, pp. 236–237.
[47] P. Milojkovic, M. P. Christensen, and M. W. Haney, "Multi-scale lens design for the global multi-chip FAST-Net interconnection module," in *Lasers and Electro-Optics Society 14th Annu. Meeting (LEOS 2001)*, vol. 2, Nov. 2001, pp. 814–815.
[48] J. J. Morikuni and S. M. Kang, *Computer-Aided Design of Optoelectronic Integrated Circuits and Systems*. Englewood Cliffs, NJ: Prentice-Hall, 1996.



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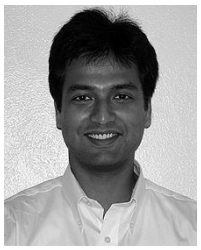
Previously, he was a Faculty Member at the University of North Carolina at Charlotte. In 1999, he joined the University of Delaware, Newark, where he is currently a Full Professor in the Department of Electrical and Computer Engineering. He has published 32 journal papers, 79 conference papers, and six patents. His research interests are in the area of mixed-signal interface circuits for photonics.

Dr. Kiamilev is a Member of the IEEE, the Optical Society of America (OSA), and The International Society for Optical Engineers (SPIE). He was the recipient of the Office of Naval Research Graduate Fellowship.



Amitava Bhaduri (M'02) received the B.E degree in electronics and telecommunication engineering from Bengal Engineering College (Deemed University), West Bengal, India, in 1997 and the M.E.E degree in electrical engineering from the University of Delaware, Newark, in 2002. He is currently working toward the Ph.D. degree in computer engineering with the University of Cincinnati, Cincinnati, OH.

He was working as a Systems Analyst with Tata Consultancy Services, India, from 1997 to 1999, where he was actively involved in a software development project. From 1999 to 2000, he was a Senior Software Engineer with Motorola, India, and was the System Administrator of a few project teams. His current research interests are in computer-aided design (CAD) for radio-frequency complementary metal–oxide–semiconductor (CMOS) circuits.

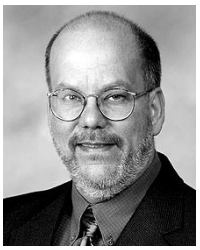
Mohammed Taufik (S'98) received the B.E. degree in electrical engineering from the Insitut Teknologi Bandung, Bandung, Indonesia, in June 2000. He is currently working toward the M.S. degree in electrical and computer engineering with the University of Delaware, Newark.

Xingle Wang, photograph and biography not available at the time of publication.

Arthur S. Morris, III (S'89–M'87) received the B.S. degrees in physics and electrical engineering and the M.S. and Ph.D. degrees in electrical engineering all from North Carolina State University (NCSU), Raleigh, in 1983, 1986, and 1993, respectively.

As a Scientist/Engineer concentrating on physical electronics and electromagnetic fields for more than 20 years, he has contributed to device technologies ranging from high-power traveling-wave tubes to millimeter-wave heterojunction bipolar transistors, and he has developed products for markets from high-voltage instrumentation to broad-band communication systems. He joined Microcosm Technologies (now Coventor) in 1999 to lead software and hardware development to support the transition of microsystems from the laboratory into products for radio-frequency (RF) and optical applications. He is currently Chief Technology Officer and Vice President of Engineering at wiSpry, Inc., a spinout of Coventor, Cary, NC, developing high-value RF products utilizing microelectromechanical systems (MEMS) and microstructures. He is also an Adjunct Professor at NCSU.

Dr. Morris is a Member of the IEEE, Phi Kappa Phi, Eta Kappa Nu, Tau Beta Pi.



James Kruchowski (M'80) received the B.S.E.E. degree with distinction from the University of Minnesota, Institute of Technology, Twin Cities, in 1980.

Upon the completion of his degree, he continued as a Scientist, researching integrated circuit (IC) process development with the University of Minnesota Microelectronics Research Center. In 1981, he joined the Solid State Electronics Division, Honeywell, to develop advanced IC processes for photolithography and plasma etching. In 1986, he joined Cray Research, Inc., to apply IC process development techniques to next-generation multi-chip modules packaging and later worked on signal integrity and circuit design for high-speed computing systems. In 1995, he joined Intel Corp., where he worked on signal integrity of high-speed signaling interfaces and high-speed serial communication interface characterization. In 2001, he joined the Special Purpose Processor Development Group, Mayo Foundation, Rochester, MN, to conduct advanced research and development of ultra-high-speed electrical and photonic communication systems. He has been granted several patents and has authored numerous technical publications and conference presentations.

Barry K. Gilbert (F'98) received the B.S. degree in electrical engineering from Purdue University, West Lafayette, IN, and the Ph.D. degree in physiology and biophysics (with minors in electrical engineering and applied mathematics) from the University of Minnesota.

He is currently a Staff Scientist in the Department of Physiology and Biophysics, the Mayo Foundation, Rochester, MN, and the Director of its Special Purpose Processor Development Group (with 43 full-time staff members). His research interests include the development of algorithms for the real-time analysis of wide-bandwidth image and signal data; the design of specialized signal-processing computers to execute these tasks; the development of computer-aided design tools to allow the timely design of high-complexity digital signal processors; the advancement of high-performance integrated circuit technologies, such as gallium arsenide and indium phosphide, which can be used to assemble very-high-performance signal processors; and the development of advanced electronic packaging technologies, such as multichip modules that will be capable of supporting digital integrated circuit-based processors operating at gigahertz system clock rates.